TAO-A.V Option Switch Settings: 1(Pulse/ICT104V/ICT104U/MDB)

Supported bill LKR 20, 50, 100, 500 4bills.

TAO-A.V dip-switch settings and functions:

	FUNCTION	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW1	SW2	SW3	SW4
	Reject LKR 20	ON											
★	Accept LKR 20	OFF											
	Reject LKR 50		ON										
★	Accept LKR 50		OFF										
	Reject LKR 100			ON									
★	Accept LKR 100			OFF									
	Reject LKR 500				ON								
★	Accept LKR 500				OFF								
	Reserved					ON							
★	Reserved					OFF							
	Reserved						ON						
★	Reserved						OFF						
	Harness Disable							ON					
★	Harness Enable							OFF					
	Inhibit Active High								ON				
★	Inhibit Active Low								OFF				
★	1 pulse / LKR 10									OFF	OFF		
	2 pulses / LKR 10									ON	OFF		
	4 pulses / LKR 10									OFF	ON		
	10 pulses / LKR 10									ON	ON		
★	Interface Timing Conversion	50ms LO / 50ms HI										OFF	OFF
		60ms LO / 300ms HI										ON	OFF
		30ms LO / 50ms HI										OFF	ON
		150ms LO / 150ms HI										ON	ON

★ Manufacture setting

◈ Note : (1) Default setting.

(2) Use 2nd and 3rd dip of the internal dip-switch to change different interface protocol.

(3) Remove the front cover and the dip-switch in on the CPU board.

(Please refer to "SW1" setting.)

Interface Settings: 2(Pulse)

	INTERFACE	SW1	SW2	SW3	SW4
★	Credit-Pulse Normal HIGH	ON			
	Credit-Pulse Normal LOW	OFF			
★	Pulse Mode		ON	OFF	
	ICT104V Interface		ON	ON	
	ICT104U Interface		OFF	ON	
	MDB Interface		OFF	OFF	
	Reserved				ON
★					OFF

★ Manufacture setting

Currency Assign Data

Interface / Bill value	ICT104U	Pulse	MDB	ICT104V
BV1	LKR 20	LKR 20	LKR 20	LKR 20
BV2	LKR 50	LKR 50	LKR 50	LKR 50
BV3	LKR 100	LKR 100	LKR 100	LKR 100
BV4	LKR 500	LKR 500	LKR 500	LKR 500

Interface Settings: 2(ICT104V)

	INTERFACE	SW1	SW2	SW3	SW4
★	Reserved	ON			
	Reserved	OFF			
	Pulse Mode		ON	OFF	
★	ICT104V Interface		ON	ON	
	ICT104U Interface		OFF	ON	
	MDB Interface		OFF	OFF	
	Reserved				ON
★					OFF

★ Manufacture setting

Interface Settings: 2(ICT104U)

	INTERFACE	SW1	SW2	SW3	SW4
★	Reserved	ON			
	Reserved	OFF			
	Pulse Mode		ON	OFF	
	ICT104V Interface		ON	ON	
★	ICT104U Interface		OFF	ON	
	MDB Interface		OFF	OFF	
	Reserved				ON
★					OFF

★ Manufacture setting

TAO-V-LKR4 Interface Settings: 2(MDB)

	FUNCTION	SW1	SW2	SW3	SW4
★	Scaling Factor (SF) = 100 Decimal Point Position (DPP) = 2	ON			
	Scaling Factor (SF) = 1 Decimal Point Position (DPP) = 0	OFF			
	Pulse Mode		ON	OFF	
	ICT104V Interface		ON	ON	
	ICT104U Interface		OFF	ON	
★	MDB Interface		OFF	OFF	
	Reserved				ON
★					OFF

★ Manufacture setting

V. 1.0 Part Number : SWM6LK410-R